"Verilog Implementation of Digital Circuit Designs on FPGA

using Vivado"

Topic: Traffic Light Controller Design using Verilog

Traffic control is a challenging problem in many cities. This is due to the large number of vehicles and the high dynamics of the traffic system. Poor traffic systems are the big reason for accidents, time losses. In this method of approach, it will reduce the waiting time of the vehicles at traffic signals. The hardware design has been developed using Verilog Hardware Description Language (HDL) programming.

Verilog designing is hardware descriptive language, the name itself suggest that it deals with the hardware designing and simulation. Basically, it becomes very difficult to mount the various electronic components on breadboard or PCB circuit. It also takes too much time for the simulation and sometimes many errors occur because of improper connection of components onto the circuit. And thus, to overcome this factor hardware descriptive language comes into conclusion. We can code the process using Verilog and we can mount it on a circuit or just upload it to the circuit accordingly so that particular circuit will work as according to the code we have written.

HDL language is often used for sequential circuits like shift register, combinational logic circuit like adder, subtractor etc. Basically it describes the digital systems like microprocessor or a memory. Whatever design that is described in HDL are independent, it has its unique state of work, very much easy to simulate, designing and debugging, and very useful than schematics, especially for large circuits thus, to overcome difficulties or problems to design the circuits manually with breadboard and PCB, use of Verilog designing in this complex world is increasing a way better. This project deals with a basic design of a T - Shaped road for traffic light control. The output of system has been tested.

**INTRODUCTION**

Traffic Lights are used to control the vehicular traffic. In the modern era, everyone has different types of vehicles resulting in rise to the numbers of vehicles. That’s why traffic lights are mandatory to avoid the traffic jams and accidents. There are three lights in the traffic signal, having different message for the drivers. Red light asks the driver to yield at the intersection, green light gives the driver free license to drive through the intersection whereas the yellow light alerts the driver to wait if the next light is red one or get ready to go / turn the engine ON if the green light is next.

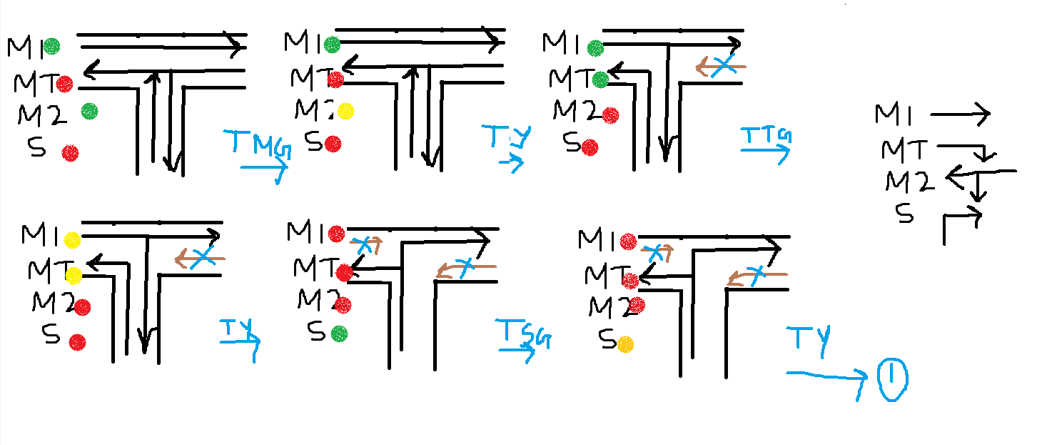
Apart from the traffic it is very necessary for the people to cross the roads at particular time interval. And this is only possible by controlling the traffic by giving some kind of signal. Analyzing the traffic, estimating the delays to the areas is crucial part. Population can be predicted using GPS trekking and thus we can easily estimate the amount of time to be taken for delay. A perfect aligning of cars, bikes, cycles, trucks with orderly flow by giving right of way, this makes the process very systematic and even in the presence of heavy traffic accident rate goes down which is one of the biggest advantage.

Timing and the delays of particular signal plays a vital role because it is very necessary for us to keep information about the amount of traffic which present in the local area. This gives us an idea about timing and delay requirement of every signal in the local area. As we know the timing depends on traffic volume and its not necessary for us to have same traffic volume at each day so for that we can estimate average volume of traffic around the local area. Average can be made with consideration of 20 days for example we will analyse the traffic of 20 days then we will take an average of it and estimate delays and timings of it. It is very necessary factor for us to have adaptive mechanism. Apart from that we can estimate the traffic volume using GPS, which can give you volume prediction every day. For this we no need to take an average of particular days. GPS give us more correct prediction of volume of traffic than calculating an average of traffic of particular days. Thus, coordinating signal timing minimizes stating and stopping of vehicles in the traffic to avoid the traffic jam.

**PROBLEM STATEMENT**

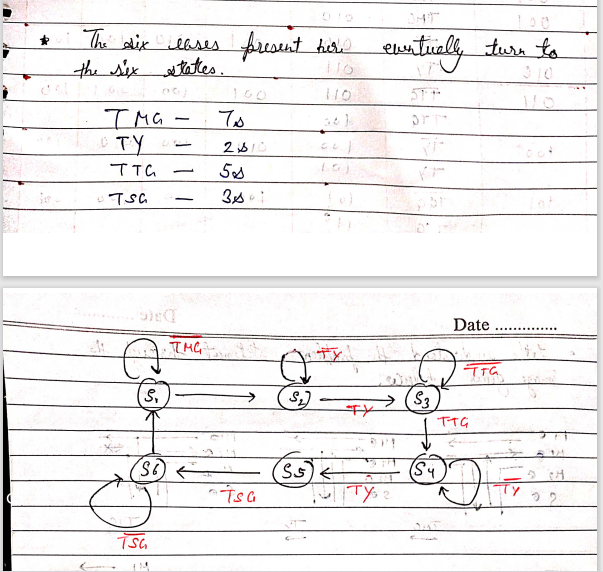
The aim of the project is to design a traffic controller for a T-intersection.

Let’s understand the problem statement through the image given below.

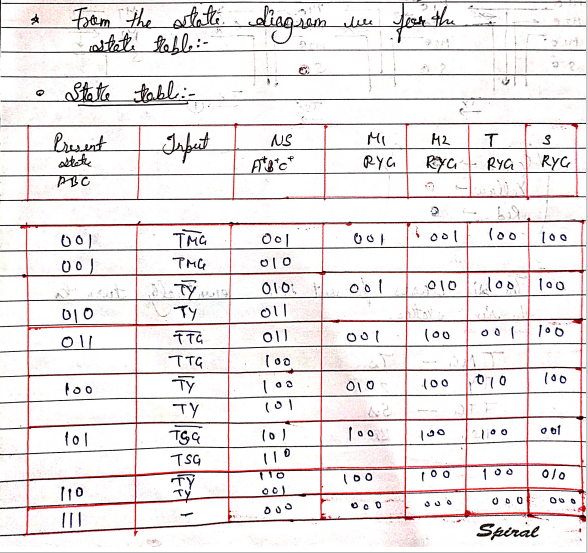


The six cases present here eventually turn to the six states.

This is the state diagram:



From the state diagram we for the state table:



**VERILOG CODE**

module Traffic\_Light\_Controller(

input clk,rst,

output reg [2:0]light\_M1,

output reg [2:0]light\_S,

output reg [2:0]light\_MT,

output reg [2:0]light\_M2

);

parameter S1=0, S2=1, S3 =2, S4=3, S5=4,S6=5;

reg [3:0]count;

reg[2:0] ps;

parameter sec7=7,sec5=5,sec2=2,sec3=3;

always@(posedge clk or posedge rst)

begin

if(rst==1)

begin

ps<=S1;

count<=0;

end

else

case(ps)

S1: if(count<sec7)

begin

ps<=S1;

count<=count+1;

end

else

begin

ps<=S2;

count<=0;

end

S2: if(count<sec2)

begin

ps<=S2;

count<=count+1;

end

else

begin

ps<=S3;

count<=0;

end

S3: if(count<sec5)

begin

ps<=S3;

count<=count+1;

end

else

begin

ps<=S4;

count<=0;

end

S4:if(count<sec2)

begin

ps<=S4;

count<=count+1;

end

else

begin

ps<=S5;

count<=0;

end

S5:if(count<sec3)

begin

ps<=S5;

count<=count+1;

end

else

begin

ps<=S6;

count<=0;

end

S6:if(count<sec2)

begin

ps<=S6;

count<=count+1;

end

else

begin

ps<=S1;

count<=0;

end

default: ps<=S1;

endcase

end

always@(ps)

begin

case(ps)

S1:

begin

light\_M1<=3'b001;

light\_M2<=3'b001;

light\_MT<=3'b100;

light\_S<=3'b100;

end

S2:

begin

light\_M1<=3'b001;

light\_M2<=3'b010;

light\_MT<=3'b100;

light\_S<=3'b100;

end

S3:

begin

light\_M1<=3'b001;

light\_M2<=3'b100;

light\_MT<=3'b001;

light\_S<=3'b100;

end

S4:

begin

light\_M1<=3'b010;

light\_M2<=3'b100;

light\_MT<=3'b010;

light\_S<=3'b100;

end

S5:

begin

light\_M1<=3'b100;

light\_M2<=3'b100;

light\_MT<=3'b100;

light\_S<=3'b001;

end

S6:

begin

light\_M1<=3'b100;

light\_M2<=3'b100;

light\_MT<=3'b100;

light\_S<=3'b100;

end

default:

begin

light\_M1<=3'b000;

light\_M2<=3'b000;

light\_MT<=3'b000;

light\_S<=3'b010;

end

endcase

end

endmodule

**TESTBENCH**

module Traffic\_Light\_Controller\_TB;

reg clk,rst;

wire [2:0]light\_M1;

wire [2:0]light\_S;

wire [2:0]light\_MT;

wire [2:0]light\_M2;

Traffic\_Light\_Controller dut(.clk(clk) , .rst(rst) , .light\_M1(light\_M1) , .light\_S(light\_S)

,.light\_M2(light\_M2),.light\_MT(light\_MT) );

initial

begin

clk=1'b0;

forever #(1000000000/2) clk=~clk;

end

initial

begin

rst=0;

#1000000000;

rst=1;

#1000000000;

rst=0;

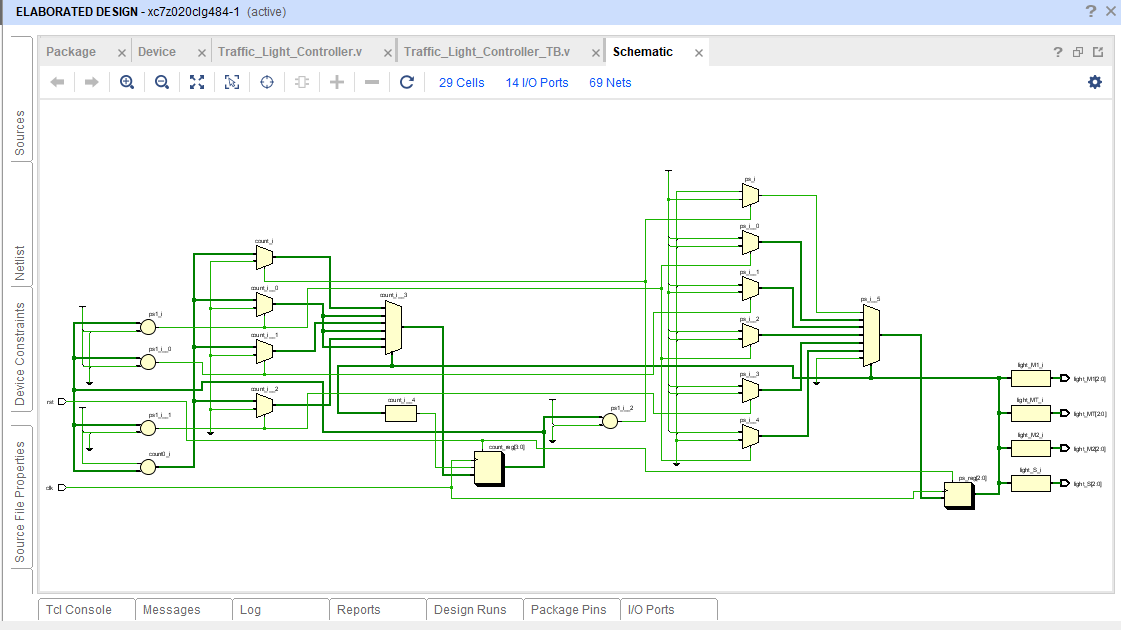
#(1000000000\*200);

$finish;

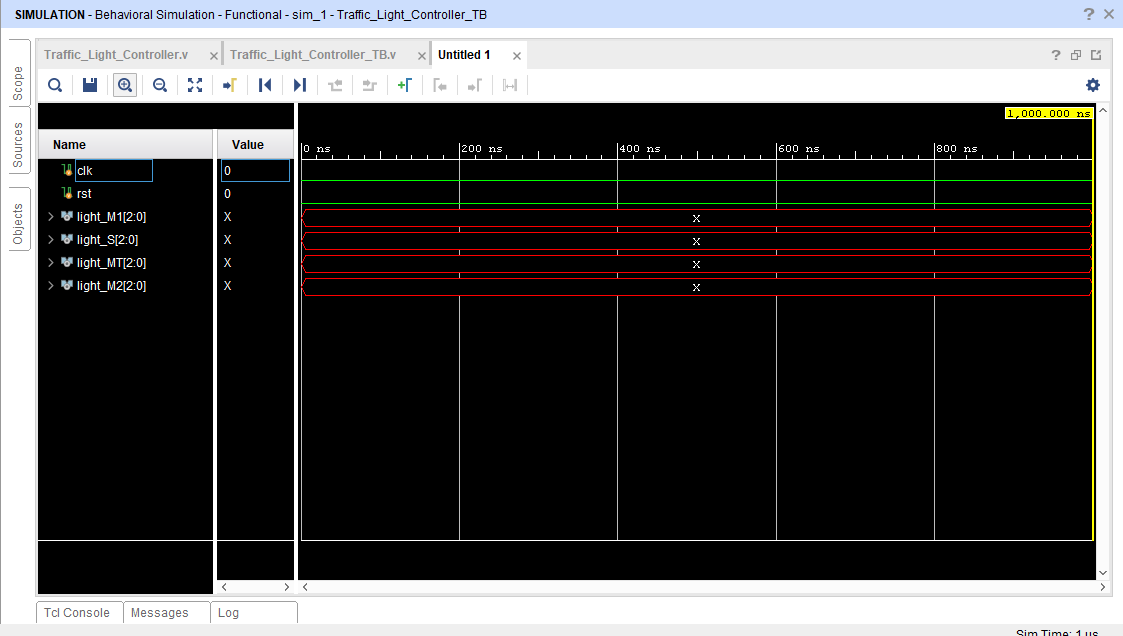
end

endmodule

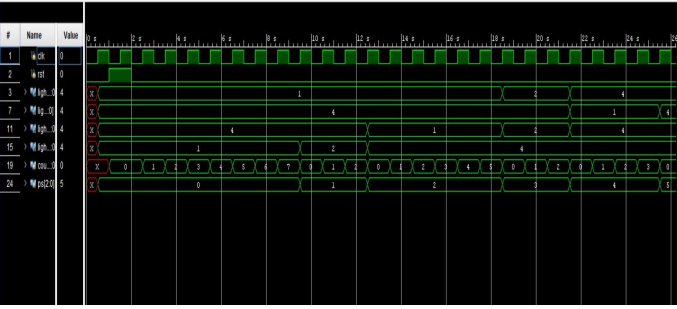
**RTL (Schematic)**

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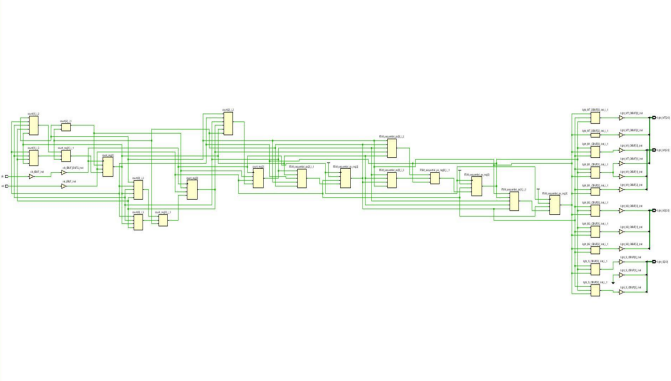
**Behavioral Simulation (Before Clock)**

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**Behavioral Simulation (After Clock)**



**SCHEMATIC AFTER IMPLEMENTATION**

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